Remarks

Claims 10, 11, 16, 18 and 25 have been amended. Claims 30 and 31 have been newly added. Reconsideration and allowance of the pending claims are respectfully requested.

Objection under C.F.R. 1.77(b)

The Office Action objected to the specification under 37 CFR 1.77(b). However, as pointed out by the Examiner, 37 C.F.R. 1.77(b) is only intended as a suggestion layout for the application and therefore not proper grounds for an objection.

Applicant kindly points out that both the MPEP § 608.01 paragraph 6.01 and 37 C.F.R. §1.77(b) do not require the presence of each of the section headings. MPEP § 608.01 paragraph 6.01 merely indicates 'The following guidelines illustrates the ***preferred*** layout for the specification of a utility application' and 37 C.F.R. §1.77(b) merely indicates 'The specification ***should*** include the following sections in order.' Accordingly, Applicant has elected not to utilize all of the suggested section headings and requests that the Examiner remove this objection.

Objection under 35 U.S.C. 112

The Office Action rejected claims 10-11 due to misspelling of 'clam' of claim 10 and virtual dependency of claim 11. Applicant has amended claims 10-11 to overcome the above deficiency.

Claims Rejections Under 35 U.S.C. 103(a) (Lee et al.)

The Office Action rejected claims 1-29 under 35 U.S.C. 103 as being unpatentable over Lee et al. (US PG-Pub no. 2002/0125879A1). Applicant respectfully requests the rejection of claims 1-29 be withdrawn for the following reasons.

As discussed in M.P.E.P 2143.03, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Claims 1-15

Claim 1 comprises a second memory module having a second memory array and a second buffer logic coupled to the second memory array, wherein **the second buffer logic** is further coupled the first buffer logic of the first memory module, and **transmits a test pattern to the first memory module to carry out a test of the first memory module** independently of the memory controller, is neither taught nor suggested by Lee et al.

Lee et al. teaches a test board to test memory devices. An embodiment of the test board, as depicted in Figs. 3 and 4, comprises two serial slots mounted with two memory devices (34 and 35) and two parallel slots mounted with the other two memory devices (36 and 38). Address/control signals from the motherboard are directly provided to the memory devices 34 and 35, but indirectly to the memory device

36 and 38 through a buffer 42. I/O data from the motherboard are directly provided to the memory devices 34 and 35, but indirectly to the memory device 36 and 38 through a buffer 43. The Office Action appears to regard reference slot 34 plus buffer 42 as the first memory module, and extension slot 35 plus buffer 43 as the second memory module.

However, Lee et al. does not teach or suggest that the second buffer logic 43 transmits a test pattern to either the first buffer logic 42 or the reference slot 34 of the first memory module to carry out a test of the first memory module. As depicted in Fig. 4, the buffers 42 and 43 respectively transmit address/control signals and I/O data to DUT 1 and DUT 2 so that the DUT 1 and DUT 2 may carry out input/output action and output data to comparator 45 which compares data provided form the motherboard with the output data from the DUT 1 and DUT 2. In view of this, buffer 43 of the second memory module does not transmit anything to either buffer 42 or the reference slot 34 of the first memory module in order to test the first memory module.

Therefore, claim 1 of the present application which requires **the second buffer logic** is further coupled the first buffer logic of the first memory module, and **transmits a test pattern to the first memory module to carry out a test of the first memory module** independently of the memory controller is patentable over Lee et al. Each of claims 2-15 include claim 1 as a base claim and is therefore allowable for at least the reasons stated above. Applicant respectfully requests the present rejection of claims 1-15 be withdrawn.

Moreover, Applicant would like to point out that claims 11 and 12 are patentable over Lee et al. for reasons as follows:

1) Claim 11 reciting **the test pattern incorporates a deliberately created error** is neither taught nor suggested by Lee et al.

The Office Action concedes that Lee et al. does not teach the test pattern incorporating a deliberately created error. Applicant respectfully submits that the test pattern recited in claim 11 is neither a concentration range nor a temperature range as regulated in *In re Aller*, 105 USPQ 233, and the test pattern incorporating a deliberately created error is not an optimization of ranges as suggested by the Examiner. Applicant believes the test pattern is not a range at all.

2) Claim 12 reciting **the test pattern transmitted by the second buffer logic to the first buffer logic passes through the third buffer logic**, is neither taught nor suggested by Lee et al.

The Office Action concedes that Lee et al. does not disclose the third buffer logic is interposed between the second buffer logic and the first buffer logic. Applicant submits that the third buffer logic of claim 12 is a key and inventive feature of the invention, and not simply the result of rearrangement.

Interposing the comparator 45 between buffer 42 and 43 and transmitting the test pattern from the buffer 42 to buffer 43 through the comparator 45 requires **modification of the operation of the system** of Fig. 4. However, Fig. 4 shows no data/signal communications between the buffers 42 and 43 or between the buffer 42 and the comparator 45 and therefore no data/signal communications going through

each of the buffers 42, 43 and 45. Furthermore, there is no motivation or reason for the worker in the art to interpose the comparator 45 between the buffers 42 and 43. The purpose of the system is to test a device (e.g., DUT 1 and DUT 2) under an actual operational environment. Therefore, the buffer 42 is used to transfer address/control signal to the DUT 1/DUT 2, the buffer 43 is used to transfer data to the DUT1/DUT2, and the comparator 45 is used to compare the data from the motherboard with the data output from the DUT1/DUT2. There are no data/signal communications between the buffers 42 and 43 or between the buffer 42 and the comparator 45 since no need to transmit address/control signal from buffer 42 to buffer 43 or 45 and no need to transmit data from buffer 43 or 45 to buffer 42.

Claims 16-24

Claim 16 recites a test logic to **initialize transmission of a test pattern to another buffer logic of another memory module** through the first point-to-point interface to carry out a test of the another memory module independently of a memory controller, is neither taught nor suggested by Lee et al.

As stated with regard to claim 1, Lee et al. teaches no data communications between buffers 42 and 43 or between buffers 42 and 45. The buffer 43 transfers the data received from the motherboard to the DUT in write mode, and the DUT further transmits the data to the buffer 45 in read mode after several operations to the data. However, buffer 43 does not initialize the transmission of the data to the buffer 45. In stead, such data transmission is initialized by the motherboard, and the buffer 43 just relays or retransmits the data. It is the motherboard but not the buffer 43 which sends

the address/control signal to the DUT to control read and write modes of the DUT, and further sends the data to the buffer 43 indicating the write mode destination. In light of this, the buffer 43 is not an initiator of the data transmission, but a relayer to relay the data from the motherboard to the DUT.

Therefore, claim 16 is patentable over Lee et al. Each of claims 17-24 include claim 16 as a base claim and is therefore allowable for at least the reasons stated above. Applicant respectfully requests the present rejection of claims 16-24 be withdrawn.

Claims 25-29

As stated above in regard to claim 12, Lee et al. does not teach or suggest there are data communications between buffers 42 and 43 or between buffer 42 and comparator 45. Therefore, Lee et al. does not teach or suggest data communications going through each of the buffers 42, 43 and 45.

In view of this, claim 25 which defines transmitting a command to the first buffer logic to cause **the first buffer logic to transmit a test pattern through the third buffer logic to the second buffer logic**, wherein the test pattern is used to carry out a test of the second memory module independently of a memory controller, is also allowable. Each of claims 26-29 includes claim 16 or 25 as a base claim, and is therefore allowable for at least the reasons stated above. Applicant respectfully requests the present rejection of claims 25-29 be withdrawn.

Claims Rejections Under 35 U.S.C. 103(a) (Perego et al.)

The Office Action rejected claims 1, 16 and 29 under 35 U.S.C. 103 as being unpatentable over Perego et al. (US PAT 6,502,161 B1). Applicant respectfully requests the rejection of claims 1, 16 and 29 be withdrawn for the following reasons.

As discussed in M.P.E.P 2143.03, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Claim 1 comprising **a second memory module having** a second memory array and **a second buffer logic** coupled to the second memory array, wherein **the second buffer logic** is further coupled the first buffer logic of the first memory module, and **transmits a test pattern to the first memory module to carry out a test of the first memory module independently of the memory controller**, is neither taught nor suggested by Perego et al.

Perego et al. teaches a conventional memory system of Fig. 2B that comprises a memory controller and a plurality of memory modules. Each of the memory modules has a buffer interfacing with the memory controller via multipoint buses. Perego et al. further teaches a new memory system of Fig. 3B that comprises a memory controller and a plurality of memory subsystems. Each memory subsystem comprises a buffer interfacing with the memory controller via a point-to-point bus.

Although Perego et al. briefly talks about testing a memory module and a buffer logic of the memory module comprises a serial interface 574 to couple signals utilized in initialization of test function (col. 3, lines 16-30 and col. 11, lines 4-15), Perego et al. does not teach or suggest any details on how to test the memory devices of a first memory module by a buffer logic of a second memory module. More specifically, Perego et al. does not teach a test pattern to carry out a test of the first memory module, a buffer logic of the second memory module to transmit the test pattern to the first memory module and the test of the first memory module independent of the memory controller.

Therefore, claim 1 is patentable over Perego et al. Applicant respectfully requests the present rejection of claim 1 be withdrawn.

For similar reasons as stated above, claim 16 which defines **a buffer logic of a memory module** comprising a test logic to **initialize transmission of a test pattern to another buffer logic of another memory module** through the first point-to-point interface to carry out a test of the another memory module independently of a memory controller, and claim 25 which defines transmitting a command to the first buffer logic to cause **the first buffer logic to transmit a test pattern through the third buffer logic to the second buffer logic, wherein the test pattern is used to carry out a test of the second memory module independently of a memory controller**, are also allowable. Applicant respectfully requests the present rejection of claims 16 and 25 be withdrawn.

Newly Added Claims

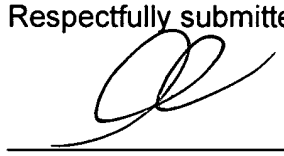
To expedite prosecution, Applicant respectfully points out in regard to claims 30-31 that neither Klein nor Perego teaches storing a test pattern in the first memory array in preparation for transmitting the test pattern from the first buffer logic to the second buffer logic, wherein the test pattern is used to carry out a test of the second memory module independently of a memory controller, as identified in claim 30.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that the application is in condition for allowance. Reconsideration is requested, and allowance of the pending claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities, which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,



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